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Attorney Docket No. 826.1767

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Kwame Osei BOATENG

Application No.: Group Art Unit:

Filed: November 5, 2001 Examiner:

For: APPARATUS AND METHOD FOR TEST-STIMULI COMPACTION

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure provisions of 37 CFR § 1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the subject application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ Form PTO-1449.
1b. ☒ Copies of IDS citations.
1c. ☐ An English language copy of search report(s) from a counterpart foreign application or a PCT International Search Report.
1d. ☒ English language translation (complete or relevant portion(s)) attached to each non-English language publication.
1e. ☐ Explanations of Relevancy of References (ATTACHMENT 1(e), hereto) for providing a concise explanation of each non-English publication.

2. ☐ In accordance with 37 CFR § 1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is

(Check appropriate Items 2a, 2b, 2c and/or 2d)

2a. ☐ satisfied because all non-English language publications were cited on the enclosed "English-language version of the search report or action which indicates the degree of relevance found by the foreign office". (See MPEP 609, Minimum Requirements for an Information Disclosure Statement, Part A(3): Concise Explanation of Relevance, pp. 600-100 to 600-101, Rev. 1, Feb. 2000.)
2b. ☐ set forth in the application.

2c. ☐ satisfied because an English language translation (complete or relevant portion(s)) is attached to each non-English language publication.

2d. ☐ enclosed as Attachment 1(e), hereto.

3. No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than search report(s) from a counterpart foreign application or a PCT International Search Report, if submitted herewith). 37 CFR §§ 1.97(g) and (h).

Respectfully submitted,

STAAS & HALSEY LLP

Dated: November 5, 2001

By: _____

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 826.1767	APPLICATION NO.
LIST OF REFERENCES CITED BY APPLICANT	FIRST NAMED INVENTOR Kwame Osei BOATENG	
(Use several sheets if necessary)	FILING DATE November 5, 2001	GROUP ART UNIT

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	AM	M. S. Hsiao and S. T. Chakradhar, "Partitioning and Reordering Techniques for Static Test Sequence Compaction of Sequential Circuits," Proceedings of the 7th IEEE Asian Test Symposium, pp. 452-457.
	AN	M. S. Hsiao and S. T. Chakradhar, "State Relaxation Based Subsequence Removal for Fast Static Compaction in Sequential Circuits," Proceedings of Design, Automation, and Test in Europe Conf., pp. 557-582.
	AO	M. S. Hsiao and E. M. Rudnick and J. H. Patel, "Fast Algorithms For Static Compaction of Sequential Circuit Test Vectors," Proceedings of IEEE VLSI Test Symposium, pp. 188-195.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	AM	I. Pomeranz and S. M. Reddy, "On Test Compaction Objectives for Combinational and Sequential Circuits," Proceedings of IEEE International Conference on VLSI Design, pp. 279-284.
	AN	S. Kajihara and K. Saluja, "On Test Pattern Compaction Using Random Pattern Fault Simulation," Proceedings of IEEE International Conference on VLSI Design, pp. 464-469.
	AO	I. Hamzaoglu and J. H. Patel, "Test Set Compaction Algorithms for Combinational Circuits," Proceedings of ACM International Conference on CAD, pp. 283-289.

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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 826.1767	APPLICATION NO. 09/985,768
LIST OF REFERENCES CITED BY APPLICANT	FIRST NAMED INVENTOR Kwame Osei BOATENG	
(Use several sheets if necessary)	FILING DATE November 5, 2001	GROUP ART UNIT 1754

U.S. PATENT DOCUMENTS

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OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	AM	K. O. Boateng, H. Takahashi and Y. Takamatsu, "Diagnosing Delay Faults in Combinational Circuits Under the Ambiguous Delay Model," IEICE Transaction on Information and Systems, Vol. E82-D, No. 12, pp. 1563-1571.
	AN	K. O. Boateng, H. Takahashi, and Y. Takamatsu, "Multiple Gate Delay Fault Diagnosis Using Test-Pairs for Marginal Delays," IEIEC Transaction on Information and Systems, Vol. E81-D, No. 7, pp. 706-715.
	AO	N. Yanagida, H. Takahashi and Y. Takamatsu, "Multiple Fault Diagnosis By Sensitizing Input Pairs," IEEE Design and Test of Computers, Vol. 12, No. 3, pp. 44-52.

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